UNIVERSITY OF WATERLOO

UW ASIC DESIGN TEAM: Cadence Tutorial

Description:

Part I: Layout & DRC of a CMOS inverter.
Part II: Extraction & LVS of a CMOS inverter.
Part III: Post-Layout Simulation.

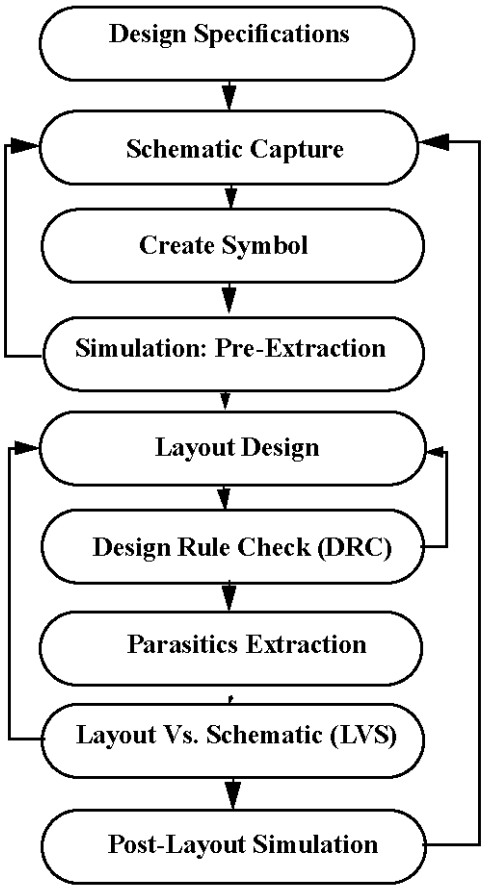
The Cadence IC design flow is depicted below.

In the first Cadence tutorial we covered the "**Schematic Capture**," "**Create Symbol**," and "**Simulation: Pre-Extraction**" steps of the IC design flow.

In Part I of this tutorial we cover the "**Layout Design**" and "**Design Rule Check (DRC)**" steps of the IC design flow.

In Part II of this tutorial we cover the "**Parasitics Extraction**" and "**Layout Vs. Schematic**" steps of the IC design flow.

In Part III of this tutorial we cover the final "**Post-Layout Simulation**" step of the IC design flow.



To proceed we will modify the schematic of our CMOS inverter to prepare it for layout:

1. First, remove all DC voltage sources from the schematic and add two new pins: VDD and VSS. Wire the VDD and VSS pins to the appropriate terminals of the CMOS inverter. Resize the NMOS channel width to 600n M.

2. Next, delete the symbol cell view and create a new symbol cell view, which will now include the VDD and VSS pins.

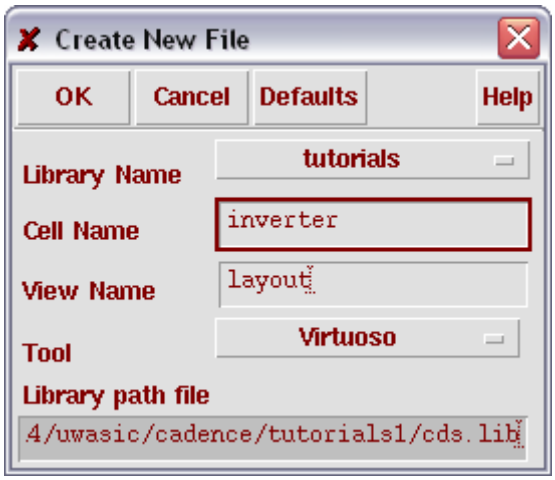
3. The new symbol will automatically appear in the *inverter_sim* schematic. Add an external power supply to the *inverter_sim* schematic and attach the external power supply to the VDD and VSS pins of the new symbol.

PART I: LAYOUT AND DRC OF A CMOS INVERTER

LAYOUT:

1. From the icfb window select: **Tools > Library Manager**.

2. In Library Manager select the *tutorials* library, the *inverter* cell, then: **File > New > Cell View**.

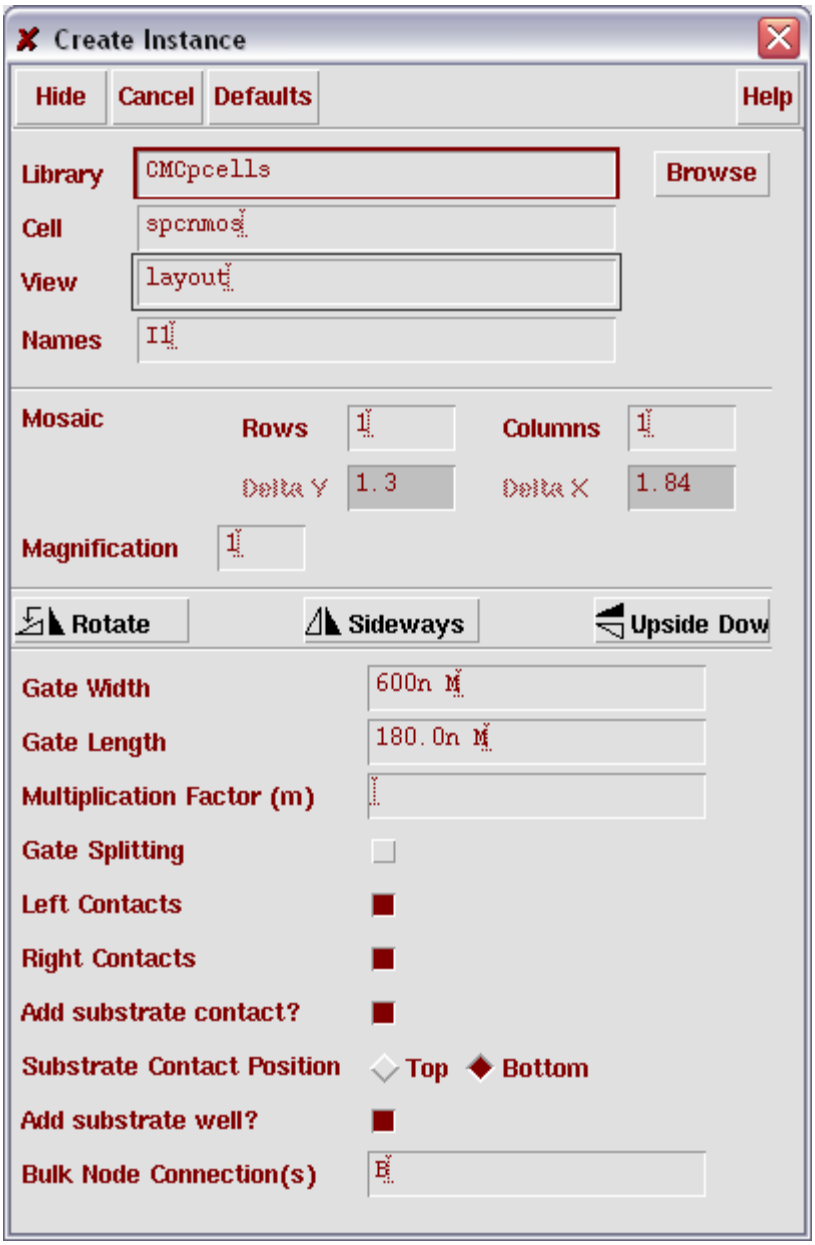


(a) In the **Tool** drop down menu select *Virtuoso*, as depicted above.
(b) Click OK.

In a few moments the LSW (Layer Selection Window) and Virtuoso® windows will appear. LSW is used to select the different materials that the CMOS inverter will be composed of. Virtuoso® is the tool in which we will draw the CMOS inverter layout.

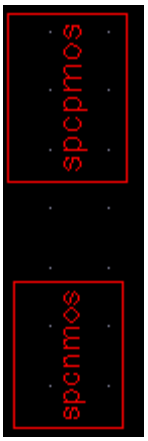
3. In Virtuoso® press "i".
In the Create Instance window click **Browse**.
In the Library Browser – Create Instance window, select the *CMCpcells* library and the *spcnmos* cell view.

As shown below, in the "Create Instance" window,
(a) Select **Add Substrate Contact?**. A **Substrate Contact Position** label appears.
(b) Select "**Bottom**" for **Substrate Contact Position**.
(c) Select **Add Substrate Well?**.
(d) You may now return to the Virtuoso® window and lay down the *spcnmos* symbol.



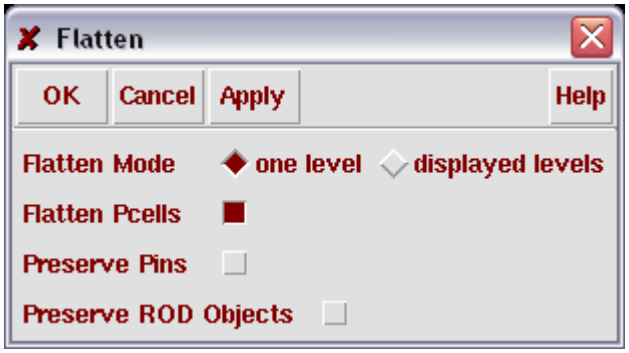
4. Repeat the step 3 to lay down an instance of the *spcpmos* symbol in Virtuoso®, only this time select **Top** for **Substrate Contact Position** and change the **Gate Width** to 800n M.

5. Organize the *spcnmos* and *spcpmos* symbols as depicted below.



6. Using the mouse, select both the *spcnmos* and the *spcpmos* symbols. Then:

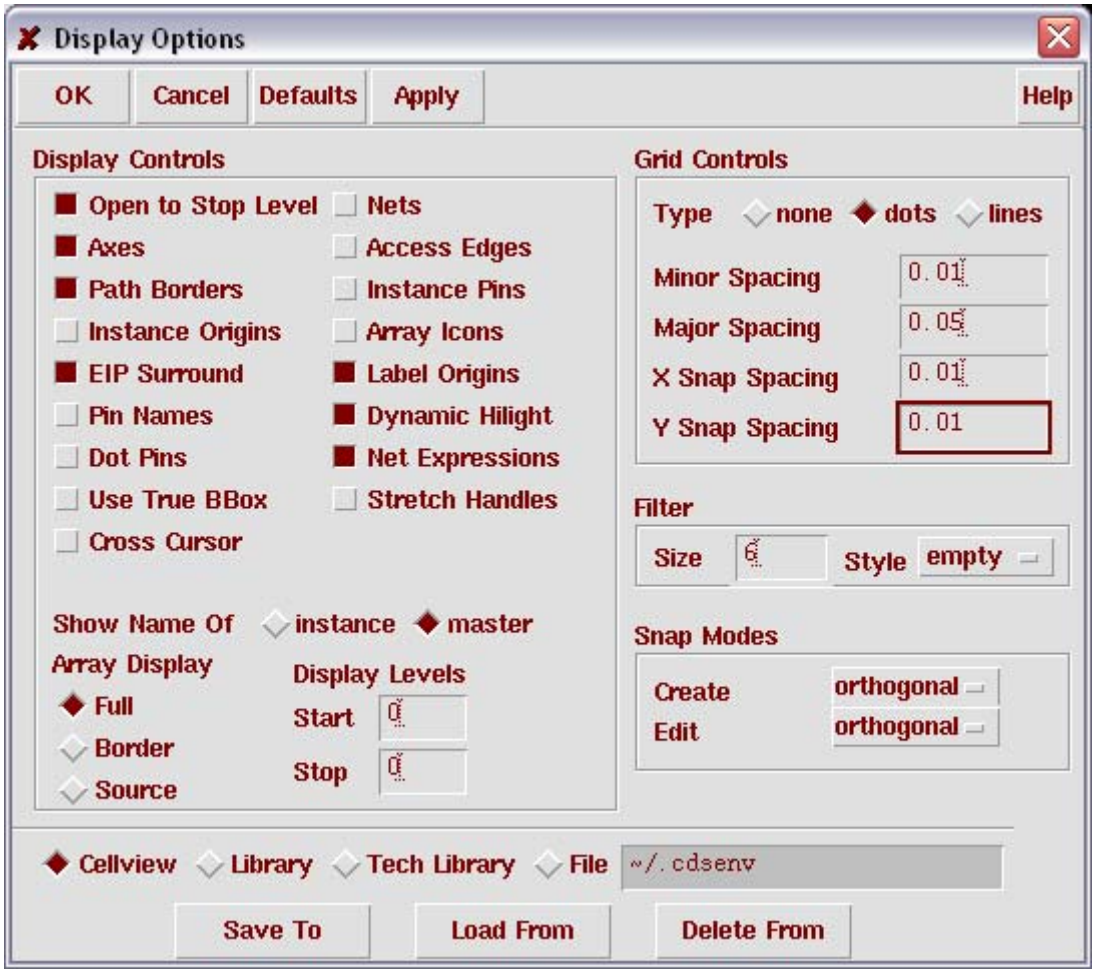
(a) Select: **Edit > Hierarchy > Flatten…**
(b) Select **Flatten Pcells**



(c) Click OK.

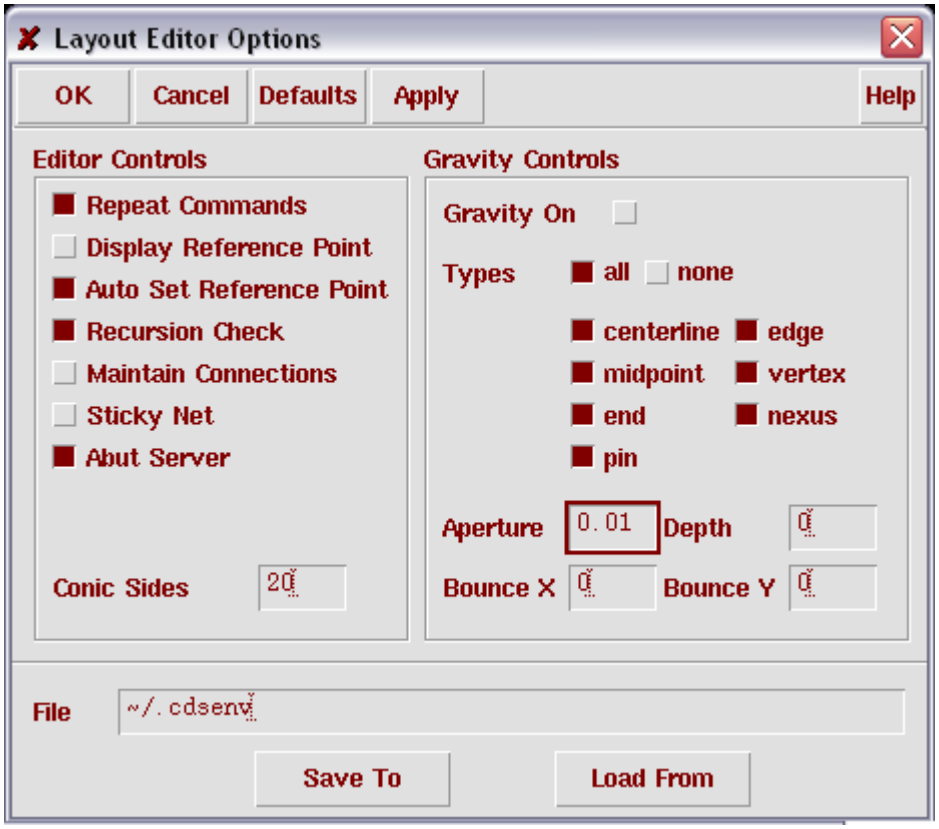
7. In Virtuoso®, select: **Options > Display**
(a) Change the **Minor spacing** to 0.01.
(b) Change the **Major spacing** to 0.05.
(c) Change the **X Snap Spacing** to 0.01.
(d) Change the **Y Snap Spacing** to 0.01.

All units are in **µm**.



(e) Click OK.

8. In Virtuoso®, select: **Options > Layout Editor**
(a) Change the **Apeture** to 0.01.



(b) Click OK.

9. **Connect the gates of the two transistors:**

(a) Use the Ruler button to mark the location of the bottom of the red poly silicon gate of the *spcnmos* symbol:


← Ruler button

(b) Delete the entire red poly silicon gate from the *spcnmos* symbol.
(c) Stretch the bottom of the red poly silicon gate of the *spcpmos* symbol using the stretch button:


← Stretch button

The red poly silicon gate should extend down to the location you marked using the ruler.

Both the *spcnmos* and *spcpmos* now share the same poly silicon gate as depicted below.

10. **Add metallization for the VDD and VSS pins**:

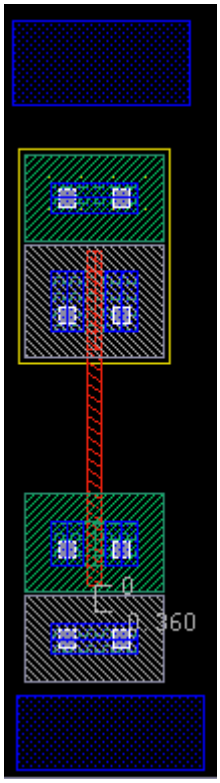
(a) Select the **metal1 | dg** material from the LSW window, and use the Rectangle button to draw two large metal1 rectangles as depicted below.

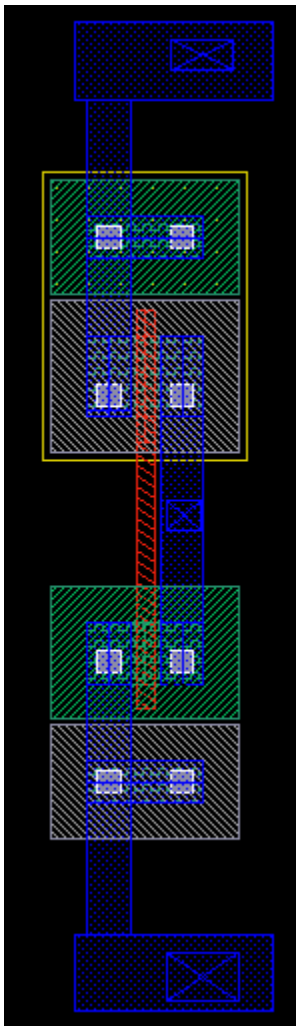

← Rectangle button

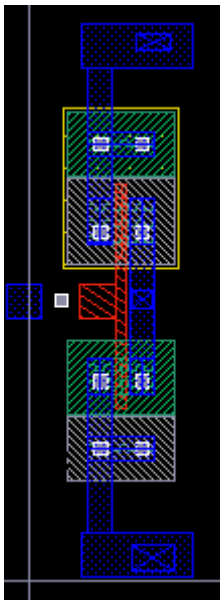
11. **Add metal interconnects:**

(a) Select the **metal1 | dg** material from the LSW window, and use the Rectangle button to draw interconnects as depicted below.

12. **Add VDD and VSS pins:**
As depicted below, a pin appears as rectangles that has an X through it.
(a) Select the **metal1 | pn** material from the LSW window.
(b) In Virtuoso® select: **Create > Pin**

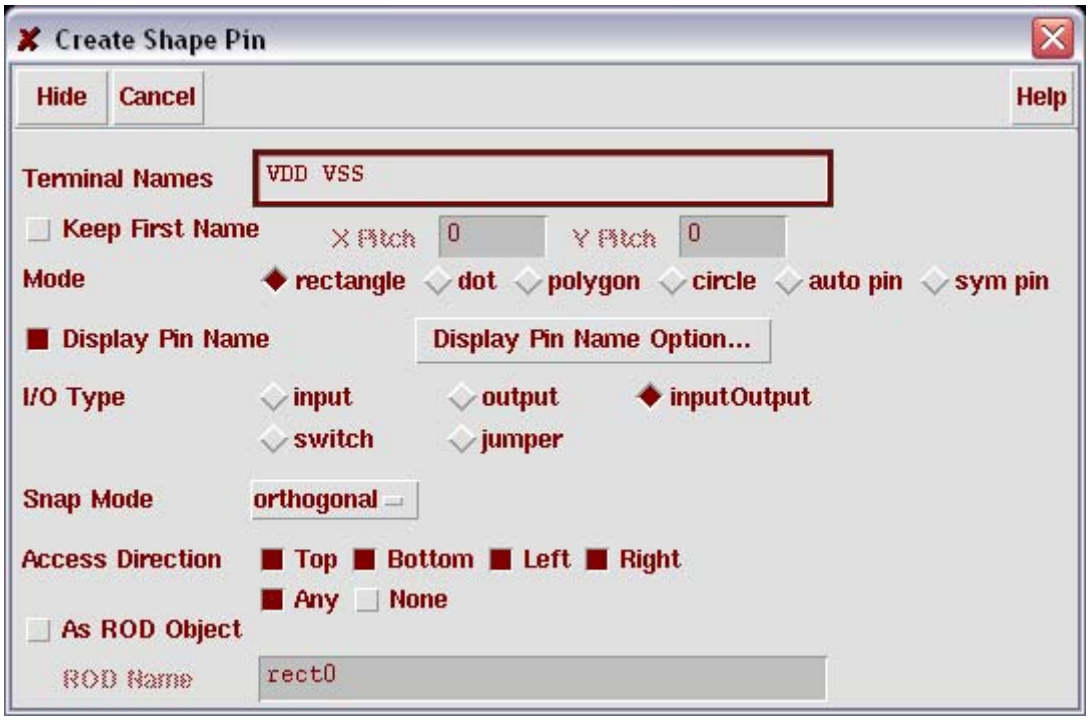

Step 9 & 10.


Step 11, 12 & 13.


Step 14 & 15.

(c) In the Create Pin Shape window:

(i) Enter *VDD* and *VSS* into the **Terminal Names** text box.
(ii) Select **Pin Shape**
(iii) Select **Display Pin Name**
(iv) Select **inputOutput**



(d) Lay down the VDD and VSS pins on the top and bottom, respectively, metallization as depicted on the previous page.

13. **Add the VOUT pin:**

Using a procedure similar to Step 12 lay down the VOUT pin on the metal interconnect that connects the two transistors, as depicted on the previous page. **NB**: Set the **I/O Type** of the VOUT pin to **output**.

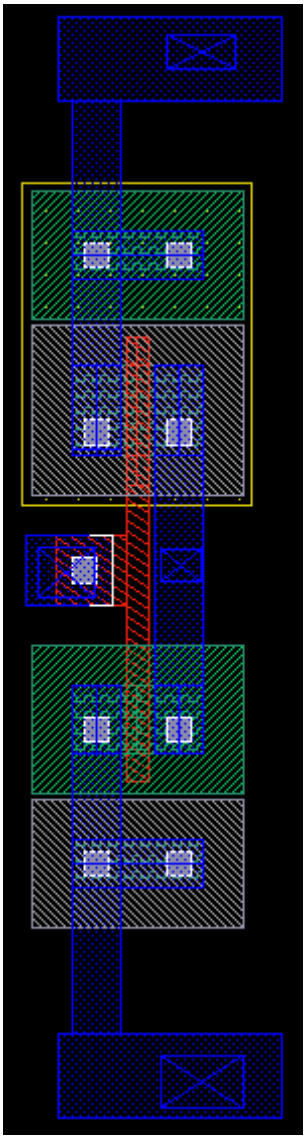
14. **Add some extra poly silicon beside the gate:**

(a) Select the **poly1 | dg** material from the LSW window, and use the Rectangle button to draw a poly silicon square as depicted on the previous page.

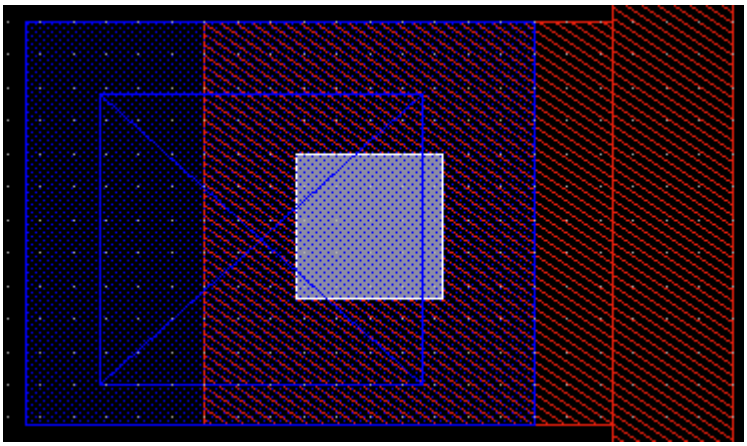
15. **Make a contact pad and metallization:**

(a) Select the **contact | dg** material from the LSW window, and use the Rectangle button to draw a 0.22 µm by 0.22 µm contact pad as depicted on the previous page.
(b) Select the **metal1 | dg** material from the LSW window, and use the Rectangle button to draw a rectangular block of metallization that is the same size as the poly silicon square that was drawn in Step 14.

16. (a) Move the contact pad and metallization, which were drawn in Step 15, onto the poly silicon square, which was drawn in Step 14, as depicted below.
(b) Add a VIN pin on top of the **poly1-contact-metal1** stack as depicted below. **NB**: Set the **I/O Type** of the VOUT pin to **input**.



Step 16.



Step 16 (close up of poly-contact-metal-pin)

The layout of the CMOS inverter is now complete.

DRC:

1. In Virtuoso® select: **Verify > DRC …**

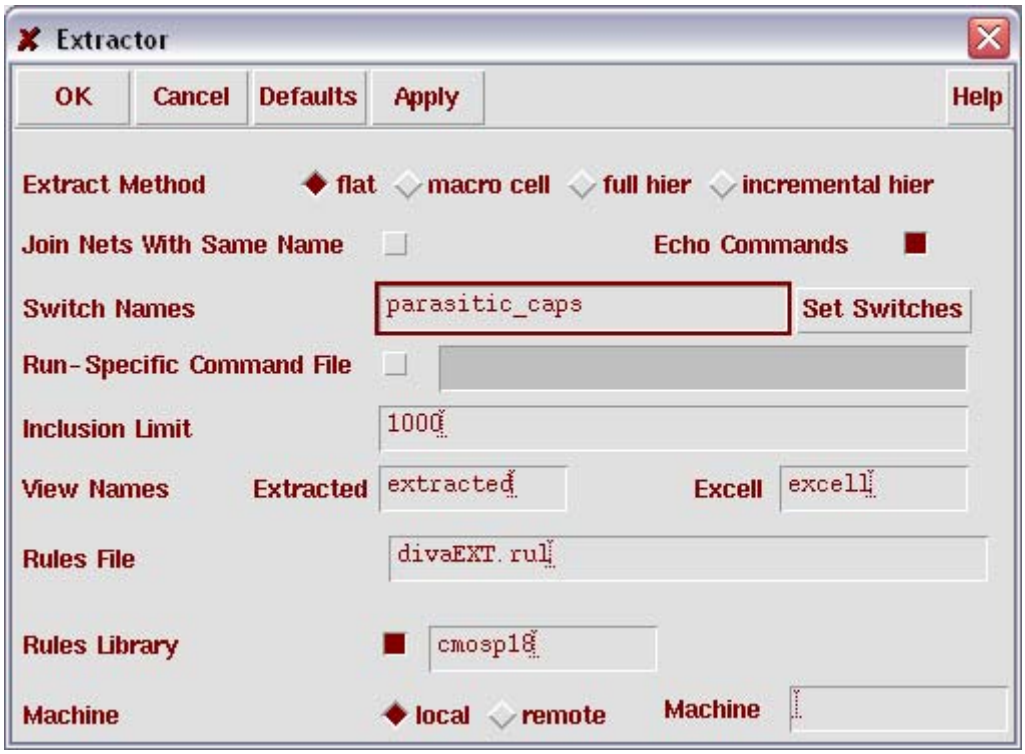
   Any errors will be reported in the icfb window. The DRC should finish with zero errors.

PART II: EXTRACTION AND LVS OF A CMOS INVERTER

EXTRACTION:

1. In Virtuoso® select: **Verify > Extract …**

   (a) Click the **Set Switches** button.
   (b) From the pop up list, select **`parasitic_caps`** and click OK.
   (c) You are now back at the Extractor window, click OK.



Any errors will be reported in the icfb window. The Extraction should finish with zero errors.

A new view, named *extracted*, will now appear in the inverter cell.

LVS:

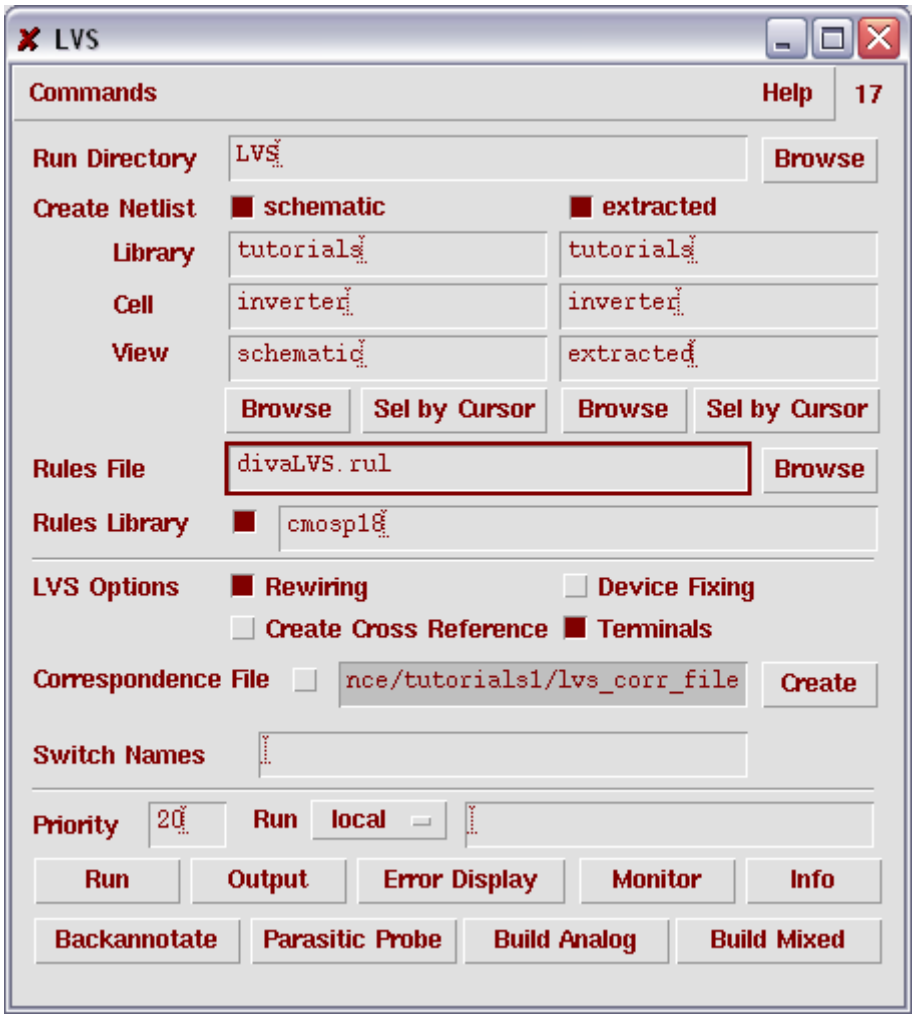
1. From Library Manager Open the *extracted* cell view.

2. From Virtuoso® select: **Verify > LVS …**

   (If an "LVS Form Contents Different" window appears select **Form Contents** and click OK)

3. In the LVS window: change the **Priority** to **20**, as shown below, and click **Run**.

   A "Analysis Job Succeeded" message will appear, click OK.



4. Though the LVS succeeded, it does not mean that the Layout matches the Schematic.

   Click the **Output** button, shown above. The si.out text file is displayed. Check the contents of the si.out text file for the following line: "**`The net-lists match`**."

   If the net-lists do not match, then there is an error in the layout. Fix the layout, and repeat the Extraction.and LVS.

   Tip: When the *Extracted* view is displayed in Virtuoso® you may toggling between Shift+f and Ctrl+f to display the devices and parasitics that were identified by the extraction.

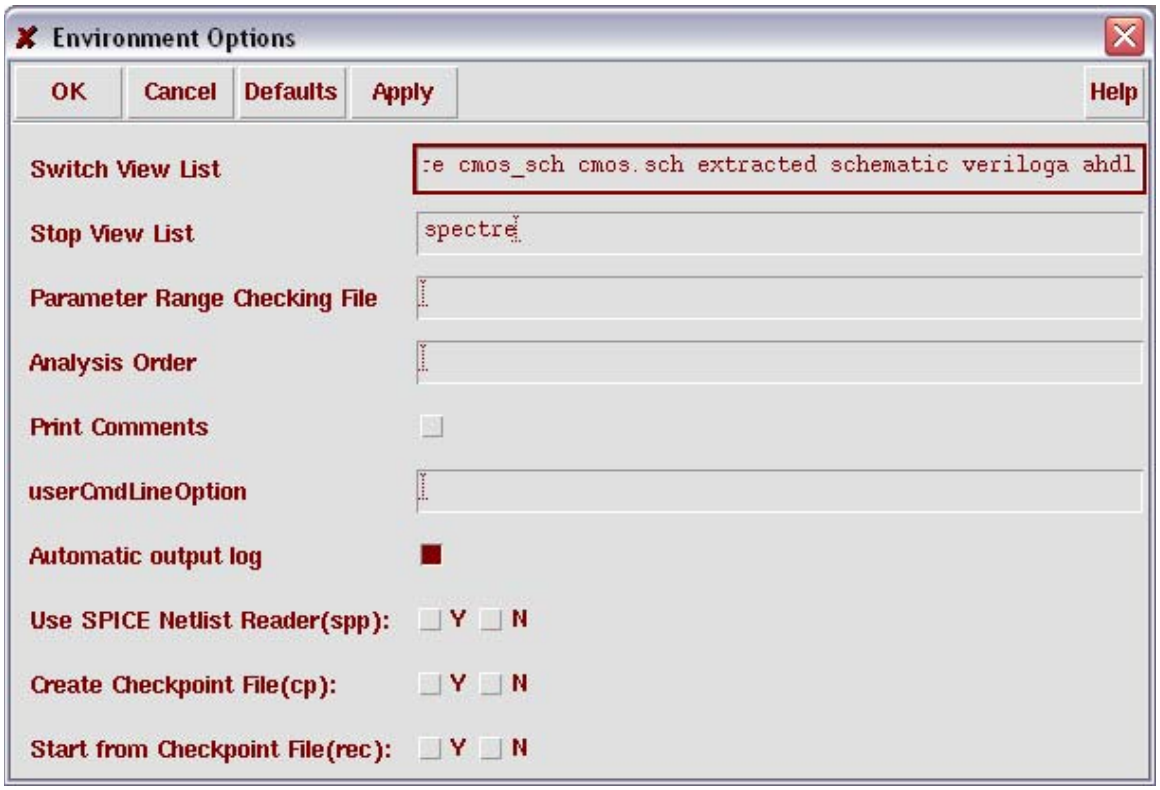
PART III: POST LAYOUT SIMULATION

1. Open the *inverter_sim* schematic.

2. In Virtuoso® select: **Tools > Analog Environment**

3. Configure Analog environment as you did in the first Cadence tutorial, then in Analog Environment select:
Setup > Environment

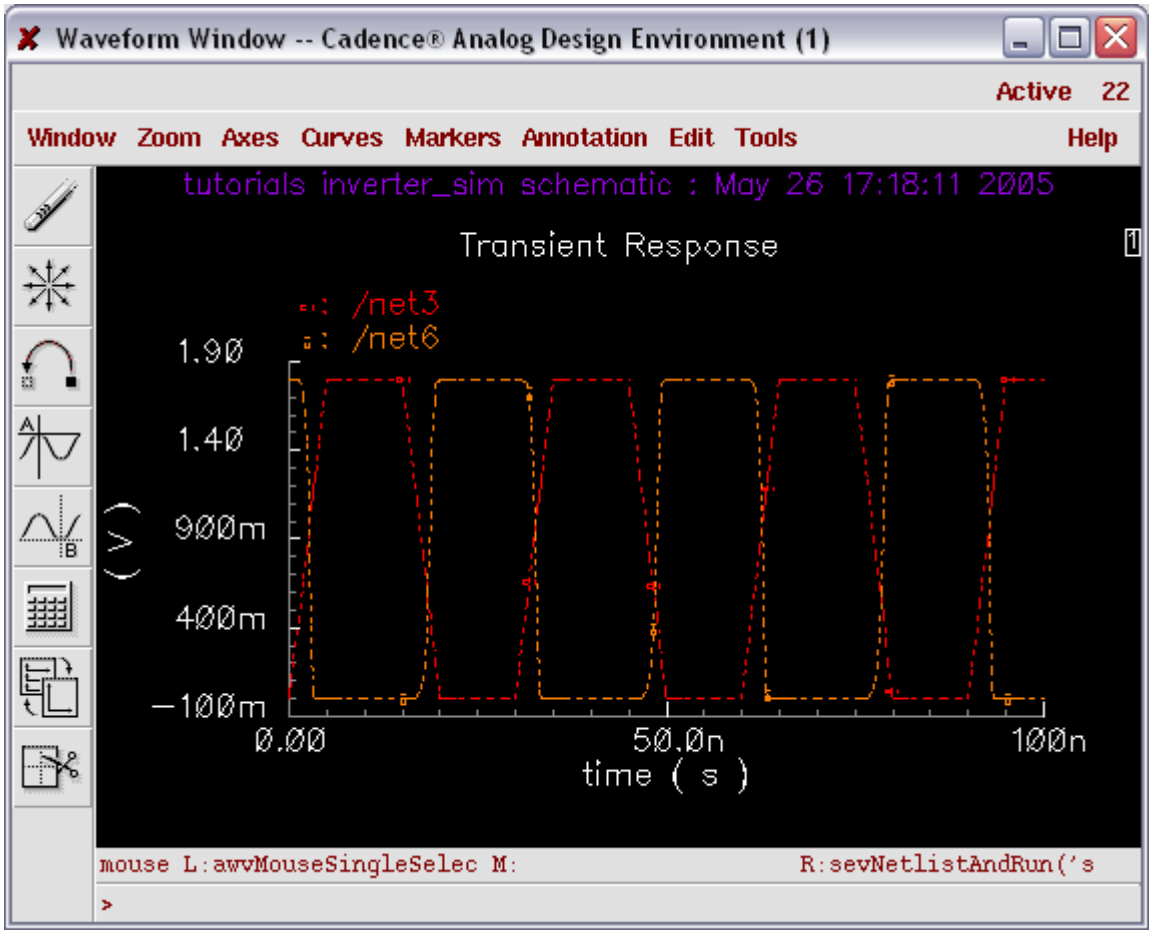
   (a) In the **Switch View List** text book type the word **`extracted`** before the word schematic as depicted below.



   (b) Click OK.
   (c) Click the Netlist and Run button.

 ← Netlist and Run button.

This simulates the extracted view of the CMOS inverter. The waveform window will be displayed as shown below.



Tip: In Virtuoso®, descend (Hot-key: e) into the *inverter* block of the *inverter_sim* schematic. You will find that the extracted view is displayed.