Projecting RASSP Benefits

James C. Anderson

Lincoln Laboratory, Massachusetts Institute of Technology*

S4-247, 244 Wood St., Lexington, MA 02173 USA

Abstract

Benefits of a RASSP-based design approach have been identified as a result of benchmarks defined and evaluated by MIT Lincoln Laboratory. One benchmark task, development of a synthetic aperture radar signal processor, serves to illustrate the effects of design trade-offs and tool usage on acquisition cost, development time and life cycle cost. Parametric cost estimation tools are used to predict the benefits of a RASSP-based design approach relative to standard practice, and one example demonstrates a factor of four cost reduction.

1: Introduction

Some goals of the RASSP (rapid prototyping of application-specific signal processors) initiative are reduction of product development time and cost, improvement of product quality and reduction in life cycle cost. Progress toward achieving these goals can be measured via costs associated with benchmark tasks assigned to the RASSP developers [1, 2]. An independent evaluation team at MIT Lincoln Laboratory, under ARPA direction, defines benchmark activities, measures progress and issues a benchmark evaluation report upon completion of each benchmark cycle. Two Lockheed Martin development teams, Sanders and Martin Marietta Laboratories, execute the benchmarks using current versions of the RASSP system. The information presented here, while based on benchmark activities related to development of a synthetic aperture radar (SAR) signal processor for an unmanned air vehicle (UAV) application [3], is not intended to represent the products or processes of either RASSP developer.

*This work was sponsored by the Advanced Research Projects Agency.

2: Cost and schedule projection methodology

Parametric cost estimation (PCE) has been selected as the methodology for establishing a nonproprietary industry standard practice baseline against which RASSP schedule and cost reductions can be compared [4]. Since success of the RASSP program will be characterized by schedule and cost reductions approaching a factor of four, an extremely accurate measurement of the RASSP process relative to standard practice is not necessarily required. PCE tools, which are claimed by their developers to provide cost estimates within 20% of actuals 70% of the time [5], are believed to provide a sufficiently accurate model of standard practice for comparison purposes.

Given sufficient time and funds, a standard practice approach to SAR processor development could have been undertaken by an independent contractor in parallel with the RASSP effort for comparison purposes. Such an approach, however, would have been costly and could only have provided a comparison of RASSP to a single standard practice effort. The PCE approach, which uses models based on historical data from a variety of projects, provided greater flexibility at less expense, and was therefore chosen in lieu of a standard practice parallel effort.

2.1: COCOMO and REVIC

COCOMO (constructive cost model, [5]) is a well-documented PCE tool for software efforts. Many computer programs that implement different versions of the COCOMO equations are available. One such program, REVIC (revised intermediate COCOMO, [6]), is of particular interest as it has been calibrated to reflect actual Air Force experience, and produces estimates close to actual costs for a variety of completed military signal processor projects [7]. COCOMO and REVIC details are presented in the appendix.

2.2: PRICE and SEER

In addition to COCOMO and REVIC, which provide only estimates for software efforts, two commercial suites of PCE tools have been used in the RASSP benchmark program. The PRICE (parametric review of information for costing and evaluation [8]) and SEER (system evaluation and estimation of resources [9]) tools provide estimates for microcircuit, hardware, hardware life cycle, design for manufacturability, software and software life cycle costs.

3: Projecting design trade-off and tool benefits

The RASSP SAR processor benchmark [10] serves to illustrate projected benefits of a RASSP design approach relative to standard practice. Examples dealing with the effects of design trade-offs and design tool usage on acquisition cost, development time and life cycle cost are presented after a brief discussion of the SAR processor requirements.

3.1: SAR processor requirements

The SAR processor requires an average computation rate of approximately one billion floating point operations per second. Specifications limit the overall chassis dimensions to 10.5” height x 20.5” length x 17.5” width, which is a size sufficient to hold a 21-slot 6U VME card cage, power supplies, fans and cabling. The average input power must not exceed 500W, resulting in 400W supplied to the cards assuming an 80% power supply efficiency. The overall chassis weight must not exceed 60 pounds, and the system must operate in ambient air temperatures ranging from 0C to 40C.

The SAR processor can be fabricated almost entirely from commercial off-the-shelf (COTS) cards. For example, Mercury MCV6 cards (or similar cards from a variety of vendors), each of which contains four 40 MHz Intel i860 processors, can provide the required signal processing capabilities. Since each card has a maximum power dissipation of 28W, up to 14 such cards could be used in the system. Also, since each card weighs 1.875 pounds, it is unlikely that a design using these cards will exceed the specified weight limit. The price of such cards [11] depends on the memory configuration, as shown in Table 1.

Table 1. Mercury MCV6

Model	Memory (Mbytes DRAM)	List Price ($)
4x4m	16	30,200
4x8m	32	35,800
4x16m	64	47,000

In addition to the MCV6 cards, a COTS backplane-mounted processor interconnect crossbar switch and a system controller card (e.g., a Motorola 68040-based MVME167), as well as a custom radar interface card, are required to complete the prototype SAR processor. Designs for the custom card, including VHDL models [2], will be available through the RASSP Education and Facilitation effort via the Internet. Given the custom card design information, the cost of purchased materials to replicate the SAR processor described here (excluding processor cards and application software) is estimated to be $100,000. In the examples presented later, this value is added to the cost of the processor cards to obtain a total hardware estimate.

The cost reductions detailed in the following examples are attributable to a RASSP-based approach involving design trade-offs and use of software development tools. The additional benefits expected from VHDL and re-use are not discussed here. Note that since the RASSP program has no effect on the cost of existing cards, such fixed costs are separated from those influenced by RASSP tools and methodology.

3.2: Standard practice design

Assume the standard practice design is produced by a hypothetical Company S (“S” for “standard practice”) with corporate structure shown in Fig. 1. The structure consists of three identifiable organizations (management, hardware and software) which communicate well with each other. Further assume that Company S is highly experienced in the production of signal processor systems for applications such as UAV SARs.

The management organization first tasks the hardware organization to produce a standard practice design. The hardware organization, through a careful and accurate analysis, determines that the entire SAR processor can be implemented using only six MCV6-4x4m cards with a 12% execution time (average MFLOPS, or millions of floating point operations per second) margin and 14% memory (Mbytes DRAM, or megabytes of dynamic random access memory) margin. Although such margins are considered small in many applications, they are not unusual for UAV applications where size, weight and power must be minimized. The resulting hardware component cost of the standard practice design is $100,000 plus the cost of six MCV6-4x4m cards, or $281,000.

The management and hardware organizations then approach the software organization to obtain an estimate of software cost and schedule for the standard practice hardware design. The software organization estimates that the application software requires 8,750 uncommented source lines of code (SLOC). Given this SLOC value and the hardware margins, the software organization uses REVIC to estimate cost and schedule (see the appendix for details). A 12% execution time margin corresponds to an 88% utilization of available execution time resources, and leads to an extra high rating for the execution time constraint. Similarly, a 14% memory margin corresponds to an 86% utilization of available memory resources, and leads to an extra high rating for the main storage constraint. With nominal ratings for all other effort adjustment factors, REVIC estimates an effort of 155 man-months and a development time of 32 calendar months. Software development cost for the standard practice design is highly influenced by the execution time and main storage constraints imposed by the hardware. REVIC estimates that the software development cost is increased by a factor of 1.66 x 1.56 = 2.59 relative to a system that uses less than 50% of its execution time and main storage resources. Since the software organization often develops code for such hardware-constrained systems, the extra software cost is routinely accepted by Company S.

Assuming a labor rate of $100 per man-hour and 152 man-hours per man-month, the total software development cost is $2,360,000. Software development is the largest expense in the project (89% for software vs. 11% for hardware) and, since the hardware consists mainly of COTS cards, the project schedule is driven by the software development schedule. The total estimated cost for the standard practice design is therefore $2,640,000 and the development duration is 32 months.

3.3: Minimum development cost RASSP design

Assume the RASSP design is produced by a hypothetical Company R ("R" for "RASSP") with corporate structure shown in Fig. 2. The structure consists of three identifiable organizations (management, hardware and software) brought together through the RASSP enterprise framework. Further assume the personnel of Company R have the same capability and experience as the personnel of Company S.

Company R investigates a variety of different designs, including the standard practice design described in Sec. 3.2. The standard practice design is identified by Company R as the COTS design that minimizes size, weight, power and hardware cost. However, since the goal of Company R is to minimize overall development cost, another design is chosen as described in the following.

Company R first performs a design trade-off to improve main storage and execution time margins by adding an appropriate number of COTS cards to the standard practice design. This trade-off reduces the software development cost by a factor of 2.59 as discussed earlier. In addition, the use of modern programming practices and software tools by Company R leads to a further software cost reduction factor, as estimated by REVIC, of 1/(0.82 x 0.83) = 1.47. The overall software development cost reduction factor is 2.59 x 1.47 = 3.8, or nearly a factor of four relative to the standard practice design. This projection assumes that all other product, computer, personnel and project attributes remain constant, and is independent of the number and organization of the software modules. The resulting software development effort estimate for 8,750 SLOC is 41 man-months ($620,000) with a development time of 21 calendar months (a factor of 1.5 reduction relative to standard practice).

The design trade-off reduces software cost but increases hardware cost. Since the standard practice design had 88% execution time utilization with six MCV6 cards, a total of (0.88 x 6)/0.5 = 10.6, or eleven cards are required to reduce the execution time utilization below 50% assuming linear scaling. Similarly, since the standard practice design had 86% memory utilization with 96 Mbytes DRAM, a total of (0.86 x 96)/0.5 = 165 Mbytes DRAM is required to reduce the main storage utilization below 50%. Since a total of 176 Mbytes DRAM is provided with eleven MCV6-4x4m cards, simply adding five cards of the same type used in the standard practice design improves the execution time and main storage margins while providing a system that is well within the specified size, weight and power constraints. The resulting hardware component cost is $100,000 plus the cost of eleven MCV6-4x4m cards, or $432,000 (a factor of 1.8 increase relative to the standard practice design).