Using an FPGA on an S-Bus Card for High Speed Serial Data Interface

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Specialized high speed data processing requires custom interface circuits to handle data rates which exceed capabilities of standard discrete logic parts. Using an FPGA realizes a savings of both power and circuit board space, and gives additional flexibility to accommodate combinations of serial or parallel interfaces with special handshaking signals.

Background

Processing image data from Earth observation satellites requires the ability to receive continuous streams of high speed serial data, Continuous data rates of 100 Mbps for 20 minutes are not uncommon. It is desired to store this incoming data in a computer for processing at a later time, Until recently, customized computer arrays or expensive data recorders were required to capture the input data. With the advent of inexpensive, high speed disk drives and powerful workstations, an inexpensive data processing system can be designed. An S-Bus adapter card which is a front end for such a data processing system using Actel's FPGA technology will be described.

System Description

A block diagram of the S-Bus adapter card is shown in Figure 1. Requirements for the adapter card include low power, small circuit board area and ability to receive continuous high speed serial data. The adapter card consists of an S-Bus controller to DMA received data to host computer disk storage, an Actel FPGA which receives high speed serial data and outputs 32 bit parallel data, and a 32 x 32 bit FIFO to buffer the input data during DMA operation.

Serial Input Data Reception

The high speed serial input data is converted to 32 bit parallel data using an Actel FPGA as shown in Figure 2. The design consists of a 32 bit serial-in-parallel-out-register (SIPO), a 32 bit output buffer register and a high speed 5 bit counter which counts the number of received bits and generates the clock enable for the output register. The FPGA also contains FIFO control logic and S-Bus control logic. The present design is implemented with a single data input channel. Additional data channels can be supported to increase the data rate while using reasonable baud rates.

Data Bit Counter

The 5 bit counter is shown in Figure 3. To obtain the highest possible performance, it is desirable to keep fanout on nets low and to use "look ahead" schemes to reduce the number of logic levels in the design. In the counter implementation, the FC2 signal goes high on the clock edge which drives Q0 and Q1 high. This technique reduces the width of the input logic driving F3. A similar technique is used for the terminal count indication (Tcn) which goes high on the clock edge which drives the counter output to 31. The terminal count is used to enable the clock on the 32 bit output register. Duplication of the terminal count signal allows the fanout on the clock enable net to be kept low for minimal delay.

Glue Logic

Interface signals for the S-Bus controller and FIFO (WR_FIFO, L_RDY, and L_HLDA) are generated in the Actel FPGA to eliminate the need for external circuitry.

Implementation Results

The serial to parallel data conversion is implemented in an Actel A1425 FPGA. This design used 28 percent of the device, Performance of the FPGA measured by the Actel Timer tool was 108 MHz using a standard speed device. The low utilization of the Actel device allows additional features to be added in future design revisions.

Conclusion

A high speed serial to parallel data converter was implemented in an Actel FPGA achieving high performance, low power and circuit board area savings. The flexibility of an FPGA in this application allows for quick design modifications to increase performance requirements or change functionality.

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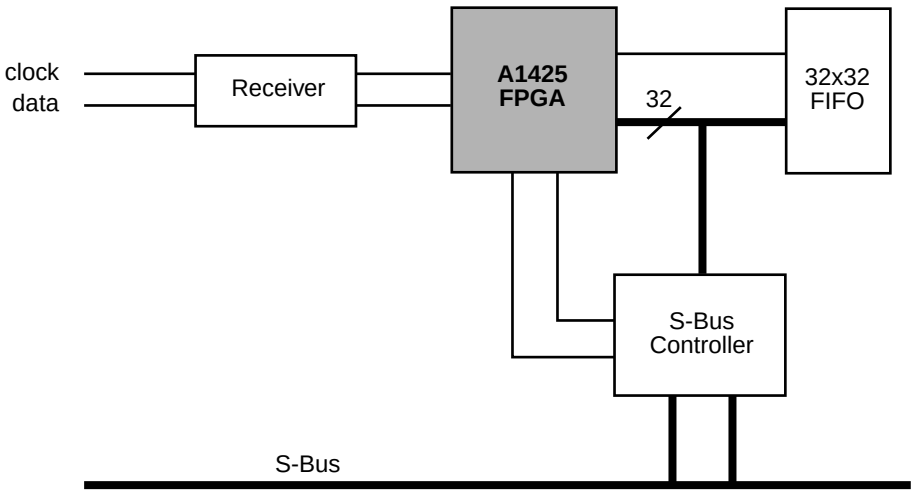

Figure 1 • *S-Bus Adapter Card*

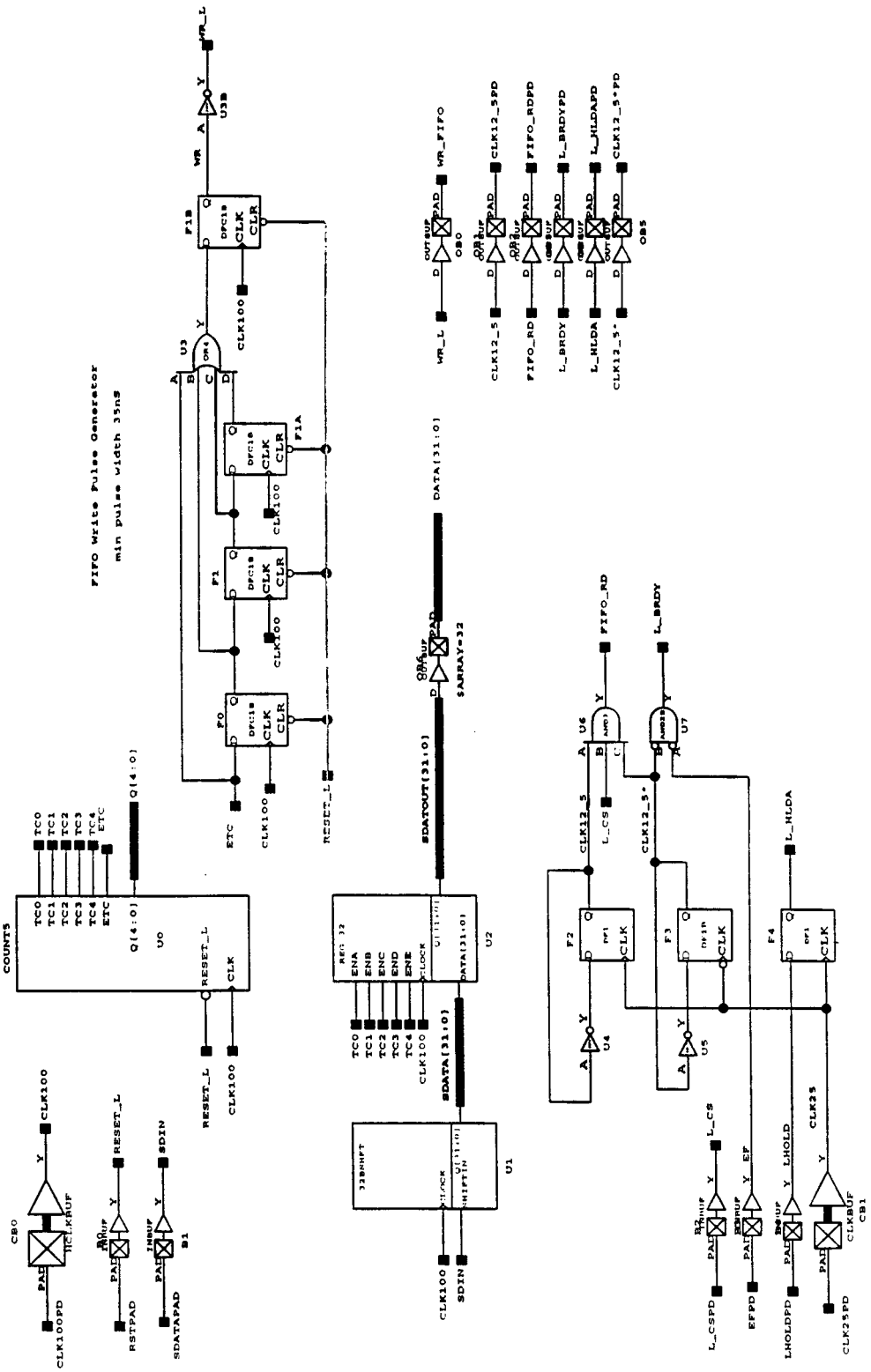

Figure 2 • *Top Level Schematic*

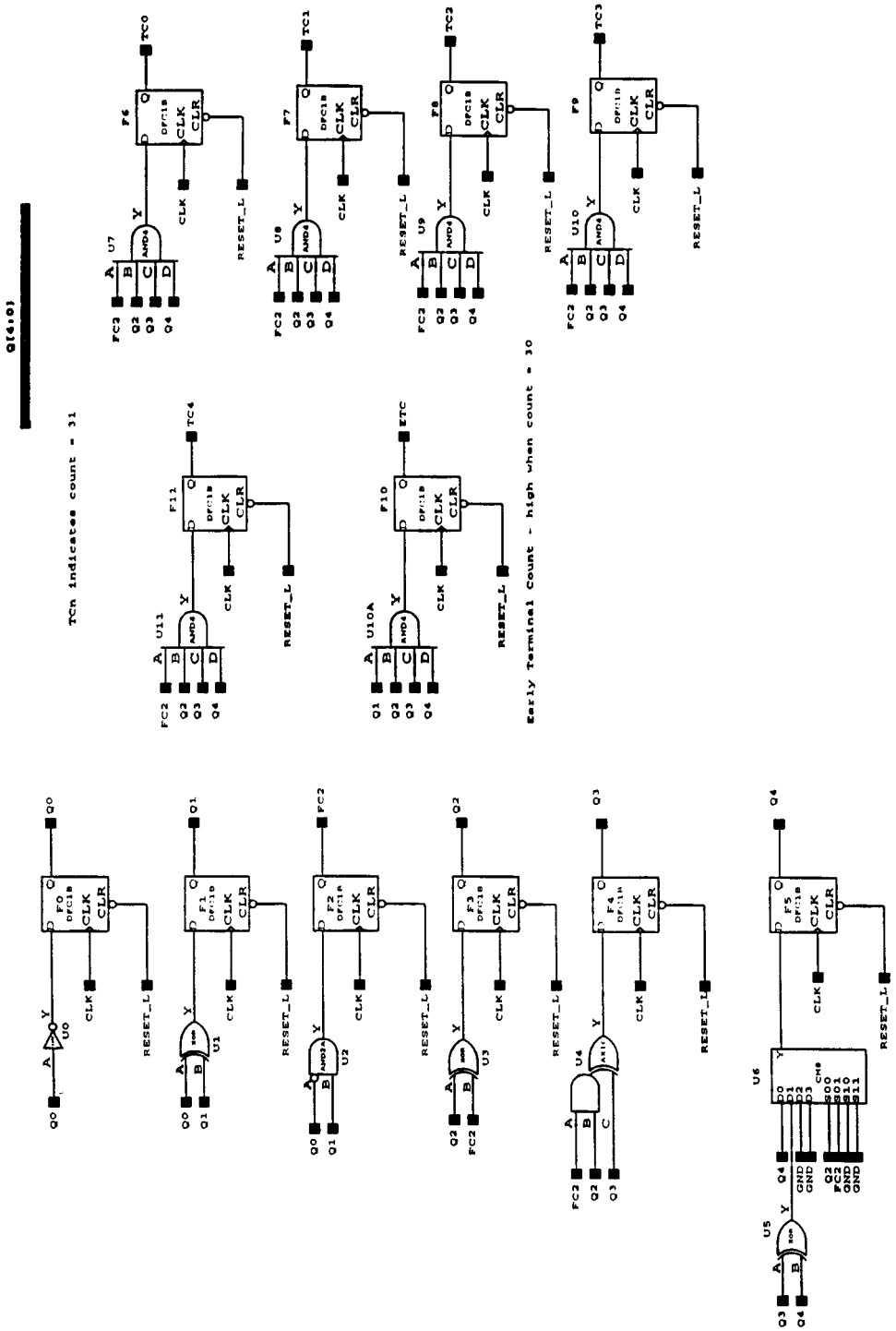

Figure 3 • *5 Bit Data Counter*