# ProASIC$^{PLUS}$ Flash Family FPGAs

FlashLock™

## Features and Benefits

### High Capacity

- 75,000 to 1 million System Gates
- 27k to 198kbits of Two-Port SRAM
- 66 to 712 User I/Os

### Reprogrammable Flash Technology

- 0.22µ 4LM Flash-based CMOS Process
- Live at Power Up, Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/ Power-Up Cycles

### Performance

- 3.3V, 32-bit PCI (up to 50 MHz)
- Two Integrated PLLs (1.5 to 240 MHz Input and 24 MHz to 240 MHz Output Ranges)
- External System Performance up to 150 MHz

### Secure Programming

- The Industry's Most Effective Security Key (FlashLock™) Prevents Read Back of Programming Bit Stream

### Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

### High Performance Routing Hierarchy

- Ultra Fast Local and Long Line Network
- High Speed Very Long Line Network
- High Performance, Low Skew, Splitable Global Network
- 100% Routability and Utilization

### I/O

- Schmitt-Trigger Option on Every Input
- Mixed 2.5V/3.3V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin Compatible Packages across ProASIC$^{PLUS}$ Family

### Unique Clock Conditioning Circuitry

- PLL with Flexible Phase, Multiply/Divide and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

### Standard FPGA and ASIC Design Flow

- Flexibility with Choice of Industry-Standard Front-End Tools
- Efficient Design through Front-End Timing and Gate Optimization

### ISP Support

- In-System Programming (ISP) via JTAG Port

### SRAMs and FIFOs

- ACTgen Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- 24 SRAM and FIFO Configurations with Synchronous and Asynchronous Operation Up to 150 MHz

## ProASIC$^{PLUS}$ Product Profile

| Device | APA075 | APA150 | APA300 | APA450 | APA600 | APA750 | APA1000 |
|---|---|---|---|---|---|---|---|
| Maximum System Gates | 75,000 | 150,000 | 300,000 | 450,000 | 600,000 | 750,000 | 1,000,000 |
| Maximum Registers | 3,072 | 6,144 | 8,192 | 12,288 | 21,504 | 32,768 | 56,320 |
| Embedded RAM Bits | 27k | 36k | 72k | 108k | 126k | 144k | 198k |
| Embedded RAM Blocks (256 X 9) | 12 | 16 | 32 | 48 | 56 | 64 | 88 |
| LVPECL | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| PLL | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Global Networks | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Maximum Clocks | 24 | 32 | 32 | 48 | 56 | 64 | 88 |
| Maximum User I/Os | 158 | 242 | 290 | 344 | 454 | 562 | 712 |
| JTAG ISP | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PCI | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Package (by pin count) | | | | | | | |
| TQFP | 100 | 100 | | | | | |
| PQFP | 208 | 208 | 208 | 208 | 208 | 208 | 208 |
| PBGA | | 456 | 456 | 456 | 456 | 456 | 456 |
| FBGA | 144 | 144, 256 | 144, 256 | 144, 256, 484 | 256, 484, 676 | 676, 896 | 896, 1152 |

## General Description

The ProASIC PLUS family of devices, Actel's second generation Flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC PLUS family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to 1 million system gates, supported with up to 198 kbits of 2-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of Flash technology allows all functionality to be live at power up. No external Boot PROM is required to support device programming. While on-board security mechanisms prevent all access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC PLUS a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC PLUS family achieves its nonvolatility and reprogrammability through an advanced Flash-based 0.22µm LVCMOS process with four-layer metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance fully compatible with gate arrays.

The ProASIC PLUS architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles™. Each tile can be configured as a flip-flop, latch, or 3-input/1-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant Flash switches allow 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a 4-level routing hierarchy.

Embedded 2-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depth and width. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The clock conditioning circuitry is unique. Devices contain two clock conditioning blocks, each with a PLL core, delay lines, phase shifts (0°, 90°, 180°, 270°), and clock multipliers/dividers, the circuitry needed to provide bidirectional access to the PLL, and operation up to 240 MHz. The PLL block contains four programmable frequency dividers, which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 4ns (in increments of 0.25ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high speed clock and data inputs.

To support customers' needs for more comprehensive, lower cost board-level testing, Actel's ProASIC PLUS devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information on the Flash FPGA implementation please refer to the *ProASIC PLUS Family Flash FPGA* data sheet.

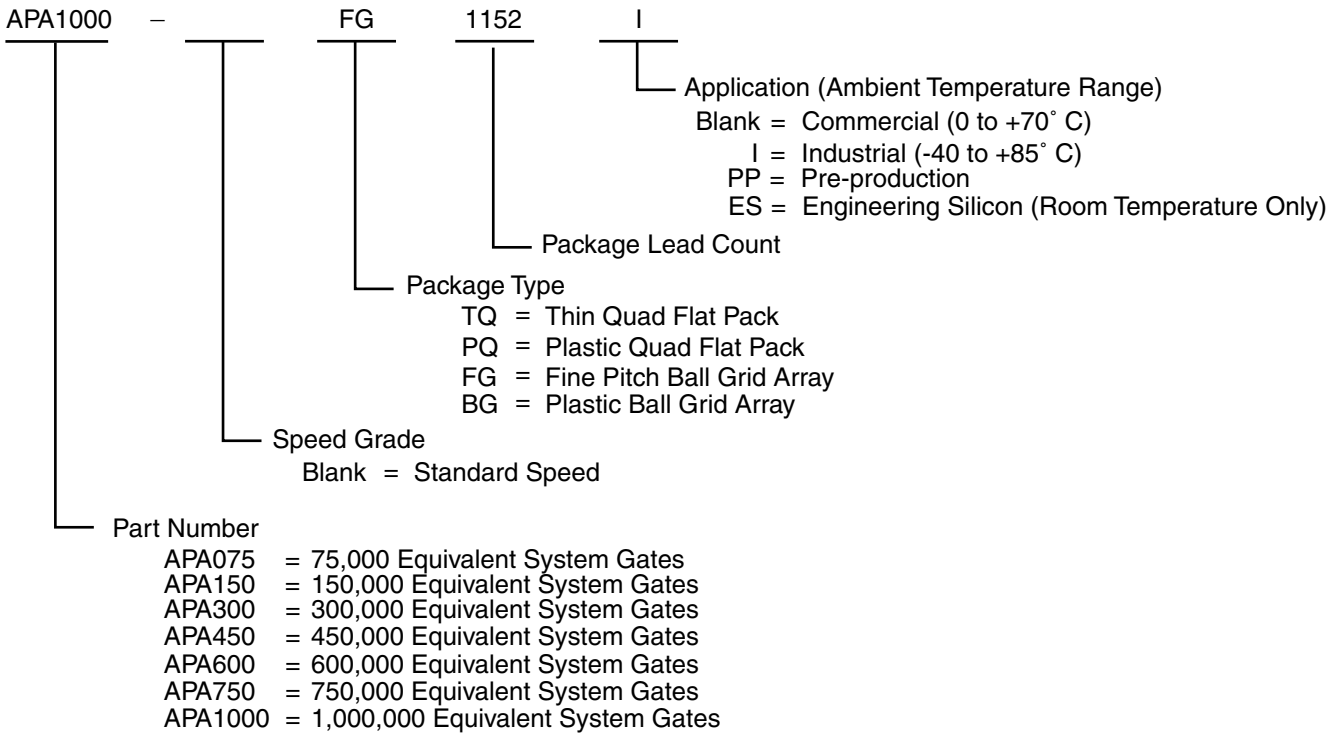
## Plastic Device Resources

| | User I/Os | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Device** | **TQFP 100-Pin** | **PQFP 208-Pin** | **PBGA 456-Pin** | **FBGA 144-Pin** | **FBGA 256-Pin** | **FBGA 484-Pin** | **FBGA 676-Pin** | **FBGA 896-Pin** | **FBGA 1152-Pin** |
| APA075 | 66 | 158 | | 100 | | | | | |
| APA150 | 66 | 158 | 242 | 100 | 186 | | | | |
| APA300 | | 158 | 290 | 100 | 186 | | | | |
| APA450 | | 158 | 344 | 100 | 186 | 344 | | | |
| APA600 | | 158 | 356 | | 186 | 370 | 454 | | |
| APA750 | | 158 | 356 | | | | 454 | 562 | |
| APA1000 | | 158 | 356 | | | | | 642 | 712 |

***Package Definitions***

*TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array*

## Ordering Information




## ProASIC^PLUS Architecture

The proprietary ProASIC^PLUS architecture provides granularity comparable to gate arrays.

The ProASIC^PLUS device core consists of a Sea-of-Tiles™ (Figure 1 on page 4). Each tile can be configured as a 3-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 2 on page 4 and Figure 3 on page 4). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash cells are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^PLUS devices also contain embedded two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking.

### Flash Switch

Unlike SRAM FPGAs, ProASIC^PLUS *uses a live on power-up ISP Flash switch as its programming element.*

*In the* ProASIC^PLUS *Flash switch*, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 2 on page 4).

### Logic Tile

The logic tile cell (Figure 3 on page 4) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra fast local and efficient long line routing resources). Any three-input, one-output logic function (except a three input XOR) can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.

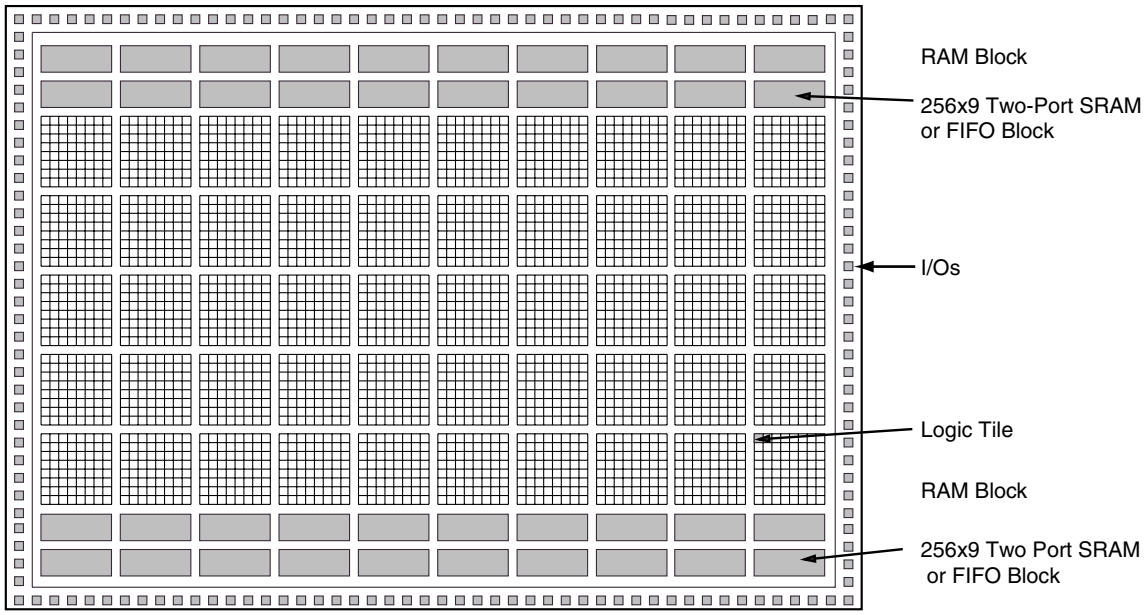



***Figure 1 •*** *The ProASIC^PLUS Device Architecture*

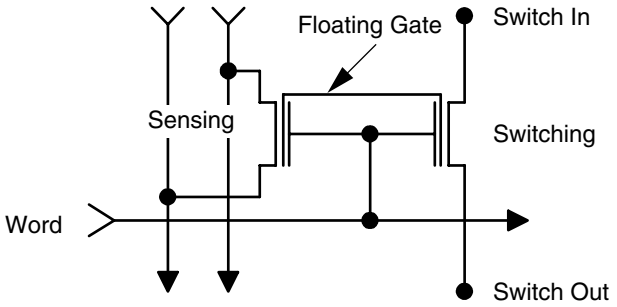



***Figure 2 •*** *Flash Switch*

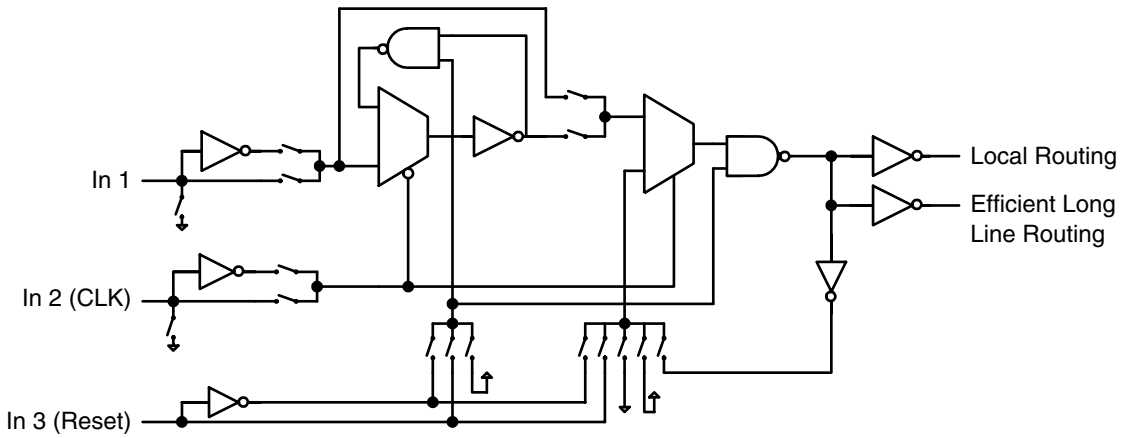



***Figure 3 •*** *Core Logic Tile*

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as “Product Brief,” “Advanced,” “Production,” and “Web-only.” The definition of these categories are as follows:

### Product Brief

The product brief is a modified version of an advanced datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Unmarked (production)

This datasheet version contains information that is considered to be final.

### Web-only

Web-only versions have three digits in the version number (example: v2.0.1). A web-only version is posted to provide customers with the latest information, but the version is not printed, because additional updates are expected shortly after posting.

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