Using FPGAs for 100 Mbit/sec Imagesetter Application

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In the magazine and newspaper industry, imagesetting speed is critical. Ten years ago, images were outputting 12 inches at 1016 dots per inch (dpi) in 5ms resulting in a peak data rate of 2.4 Mbits/s. Today's imagesetters output 18 inches or more at resolutions exceeding 2540 dpi. Peak data rates of 100Mbits/sec are now necessary.

The speed of imagesetters as well as many other business machines follows the trend of computers, lower cost, and higher speed. The FPGA facilitates the design in both regards. The cost of a design is directly related to the complexity, and increased speed adds to the complexity of producing a reliable printed circuit board (PCB). So any tools or devices that can aid the engineer in completing a complex design are welcome. Designing with the FPGA is made easier with the use of new computer aided design tools and speed is only a matter of selecting an FPGA that meets the design requirements. A wide variety of FPGA parts are available whether the speed requirements are for fast pin to pin delays, or fast internal clock and propagation delays.

FPGAs allow designers to continue meeting the high speed requirements without switching to GaAs or ECL technologies. Wide counters, registers, address, and data paths can be the most difficult to implement in a fast design. Incorporating these critical functions (such as a 16+bit counter running at 100 MHz) on one IC eliminates most of the more difficult high speed design issues usually encountered at the PCB level. Design issues such as: clock distribution, propagation delay, transmission line effects, and power supply noise are all significantly reduced for an FPGA design. If a design can be implemented with clear and predictable performance the amount work required between design and production is minimized.

With continued shrinking time to market cycles and the need to remain competitive, logic designers are constantly looking for methods to maximize the performance of current technologies. One way to do this is to make use of the FPGA, incorporating large amounts of circuitry into one package. Reductions in PCB size and power consumption can also be realized when designing with the FPGA. Programmability makes the design flexible, the tools make the designs easy to implement, and the current speeds of the FPGA make it a logical choice for high speed designs.

FPGAs were first used at ECRM in the original design of a 50 MB per second imagesetter. At the time the major purpose of the FPGA was to consolidate the design onto a single PCB of reasonable size and cost. Speed was of secondary concern as host computers could not support much more than 50 MB per second even if the imagesetter could. Faster systems were much larger and required high performance dedicated host computers to support the higher data rates. In time the speed of host computers would increase and the cost would decrease. One only had to watch the trend of computers to know the future of all related equipment.

The new imagesetter design did not require an excessively large number of gates but did have a speed requirement that was originally thought not to be possible with existing FPGA technology. Originally the design used a 50 MHz data path and a 100 MHz synchronization circuit. The new design was specified to be 2 times the speed of the original. This meant that the data path would be 100 MHz and the synchronization circuit would be 200 MHz. Since 200 MHz was not possible with any existing CMOS technology the alternatives (ECL or GaAs) were not very attractive. This portion of the circuit would definitely have to be replaced. The data path was considered optimized for a theoretical 60 MHz using a 75 MHz FPGA. If the same ratio applied to the new design the data path would need a part specified to 160 MHz, also not available in CMOS at the start of this project. Only preliminary data was available for parts approaching that speed. If only we could make the data path run at the 105 MHz rate.

With Actel being the source of the original data path design we decided to reevaluate the possibility of using Actel parts in the new design. The highest speed grade of the size part required was 105 MHz. All we had to do was fit the existing design into the new speed grade and be able to achieve better than 95% of the manufacturers specified speed limit. Timing measurements showed the original design would not run at the rated speed and would have to be redesigned, or replaced. The data sheets as well as some very helpful application notes in the Actel data books indicated the design could be made to operate at the rated speed of 105 MHz. We decided to test the manufacturer's specifications and see how fast we could make the 75 MHz part operate. If we could get the critical parts running at the maximum speed in the standard parts we would gain the confidence needed to pursue the design using the highest speed grade.

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There were many parts in the data path that required tweaking for speed but three in particular needed a new design approach; a 16 bit up counter, a 4 bit counter/synchronizer and an 8 bit shift register. Functionally each piece did not require a great deal of thought. It was the speed requirement that made the design more difficult. The two counters had to be capable of running at the limits of the rated speed without fail even under a battery of stress tests. The circuit would have to be subject to extreme variations in both power supply rails, and operating temperatures and still perform to the design specifications. With these limits in mind we made or first attempt at optimizing the critical functions.

We used the Viewlogic schematic capture package to enter the design and through the combination of Actel's design tools and Viewlogic's simulation we were able to simulate the design timing. After a few attempts at simulation we felt we had a design that would perform as required. System tests at this point did not quite reach the limit of the device specification but were far beyond the speed attained in the original design. After a more detailed performance analysis we determined there was still some room for improvement. Logic levels where reduced further and routing delays where trimmed using redundant logic. Being extremely thorough in the analysis and maximizing the capabilities of all the available tools proved to be worth all of the effort. One more simulation and we were back to system testing. This time we were able to run the standard speed device right up to the specified limit of 75 MHz. Under high temperature and low power supply voltage the device performed reliably right up to the maximum rating.

The counter is a 16 bit up counter with synchronous load, and clear. It is primarily based on the application note "Implementing Load Latency Fast Counters with ACT 2 FPGAs", Actel FPGA Data Book and Design Guide, 1994, page 9-43. The two LSB's of the counter are the fastest part of the design as they must toggle at the highest rate. Therefore the choices for implementation are limited. Also if the counter is more than four bits the lower two must be duplicated to keep the routing delays at a minimum. The Q0 bit must have feedback from the Q output with zero levels of logic to be able to toggle at the period of 1/fmax. The feedback becomes a select line to a mux that puts the inverted logic level at the D input to the flip-flop before the next clock edge. Actel provides macros that implement this type of function with effectively zero levels of logic needed for the mux portion. The toggle rate is then defined as; the Tsu (setup time of the flip-flop) plus the Tco (clock to output delay of the flip flops pad to pad).

With a high speed data path design in place all that was left was to fit the design into the higher speed grade part. It was now time to design the clocking and synchronization circuit for without a high speed clock we would not have a high speed design no matter how fast the parts we used.

We came up with a method of synchronizing the system with a 1x clock instead of the 2x or 200 MHz clock. For this we chose a device that had faster pin to pin delays as we would have to use feedback around the part for synchronization. After prototyping the design we were ready to test the performance of the 105 MHz design. System tests now proved the performance of the design right up to the maximum 105 MHz. Timing simulation results closely matched the manufacturer's specifications and the actual performance matched the simulation. Current FPGA technology is capable of performance levels that can satisfy almost any requirement. A system design engineer need only be aware of the products that are available and be able to determine when and where to apply them.

Biography

Thomas A. Everett, Electronic Design Engineer, ECRM Trust, Tewksbury, MA. I have been with the engineering group at ECRM for nine years helping to develop imagesetters for the newspaper and magazine industry. I have contributed at least in some part to all aspects of design work at ECRM including, optics, mechanics, digital and electronic design. I have most recently been assigned the task of increasing the speed of existing product lines to keep up with todays customers high speed requirements.